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Low-Noise Chopper-Stabilized Multi-Path Operational Amplifier with Nested Miller Compensation for High-Precision Sensors

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Abstract: This paper presents a low-noise multi-path operational amplifier for high-precision sensors. A chopper stabilization technique is applied to the amplifier to remove offset and flicker noise. A ripple reduction loop (RRL) is designed to remove the ripple generated in the process of up-modulating the flicker noise and offset. To cancel the notch in the overall transfer function due to the RRL operation, a multi-path architecture using both a low-frequency path (LFP) and high-frequency path (HFP) is implemented. The low frequency path amplifier is implemented using the chopper technique and the RRL. In the high-frequency path amplifier, a class-AB output stage is implemented to improve the power efficiency. The transfer functions of the LFP and HFP induce a first-order frequency response in the system through nested Miller compensation. The low-noise multi-path amplifier was fabricated using a 0.18 μm 1P6M complementary metal-oxide-semiconductor (CMOS) process. The power consumption of the proposed low-noise operational amplifier is 0.174 mW with a 1.8 V supply and an active area of 1.18 mm². The proposed low-noise amplifier has a unit gain bandwidth (UGBW) of 3.16 MHz, an input referred noise of 11.8 nV/ $\sqrt{\text{Hz}}$, and a noise efficiency factor (NEF) of 4.46.

Keywords: low-noise amplifier; chopper stabilization technique; ripple reduction loop (RRL); notch; multi-path amplifier; class AB output; noise efficiency factor (NEF)

1. Introduction

With the development of smart devices for Internet of Things (IoT), various sensor applications are becoming increasingly necessary. Among them, micro-electro-mechanical system (MEMS) sensors are receiving particular attention due to their small size, high signal-to-noise ratio (SNR), and low cost [1–4]. Sensing diminutive signals with a small output current and small output voltage amplitude using MEMS sensors requires large amplification. Therefore, high gain, high input impedance, and low-noise operational amplification are essential for various sensor interfaces [5–7]. To reduce output noise, chopper stabilization or auto-zeroing techniques are typically used [8]. The auto-zeroing technique typically operates using two phases. The first phase stores flicker noise and offset in the auto-zero capacitor, and the next phase subtracts the stored flicker noise and offset from the input signal. Because of these two phases, the auto-zeroing technique performs discrete-time operation. In addition, auto-zeroing techniques cause switching noise as well as noise folding of high-frequency components due to sampling operations, thus chopper-stabilized architecture is preferred for low-power and

low-noise continuous-time applications [9]. Chopper stabilization techniques modulate the offset and flicker noise with a chopper frequency (f_{chop}), leaving only thermal noise in the base band. However, the offset and the flicker noise are up-modulated, and these up-modulated noise signals are referred to as ripple. To attenuate this ripple, the ripple reduction loop (RRL) was proposed [10]. RRL integrates the generated ripple voltage at the output node and feeds back the integrated ripple to the input stage negatively. However, there is a limit in bandwidth because the transfer function of the amplifier produces a notch at the chopper frequency.

The bandwidth is increased by using a multi-path structure—a combination of a low-frequency path (LFP) and a high-frequency path (HFP). The transfer functions of the LFP and HFP induce a first-order frequency response in the system (a first-order system) by applying nested Miller compensation [11]. In the HFP, a class-AB output stage is implemented to improve the power efficiency. The proposed low-noise multi-path operational amplifier was fabricated using a 0.18- μm 1P6M complementary metal-oxide-semiconductor (CMOS) process. The average current consumption is 96.7 μA and the active area is 1.18 mm^2 . The proposed low-noise multi-path amplifier has a unit gain bandwidth (UGBW) of 3.16 MHz, an input referred noise of 11.8 $\text{nV}/\sqrt{\text{Hz}}$, and a noise efficiency factor (NEF) of 4.46.

2. Circuit Implementation of the Proposed Operational Amplifier

2.1. Architecture of the Proposed Multi-Path Operational Amplifier

The basic schematic is shown in Figure 1. The proposed circuit consists of two main paths, the HFP and LFP. In Figure 1, the red line represents the HFP and the blue line represents the LFP. The LFP consists of four stages, and the HFP consists of two stages. The LFP applies chopper stabilization to decrease the offset and flicker noise, while ripple is suppressed by the RRL. Connect the output of A_6 in the current adder opposite to the output of A_2 to suppress the ripple. The HFP has a first-order frequency response with one dominant pole caused by C_{m1} and the LFP has a second-order frequency response with two dominant poles caused by C_{m1} and C_{i1} . Nested Miller compensation is applied to smoothly combine the two frequency responses.

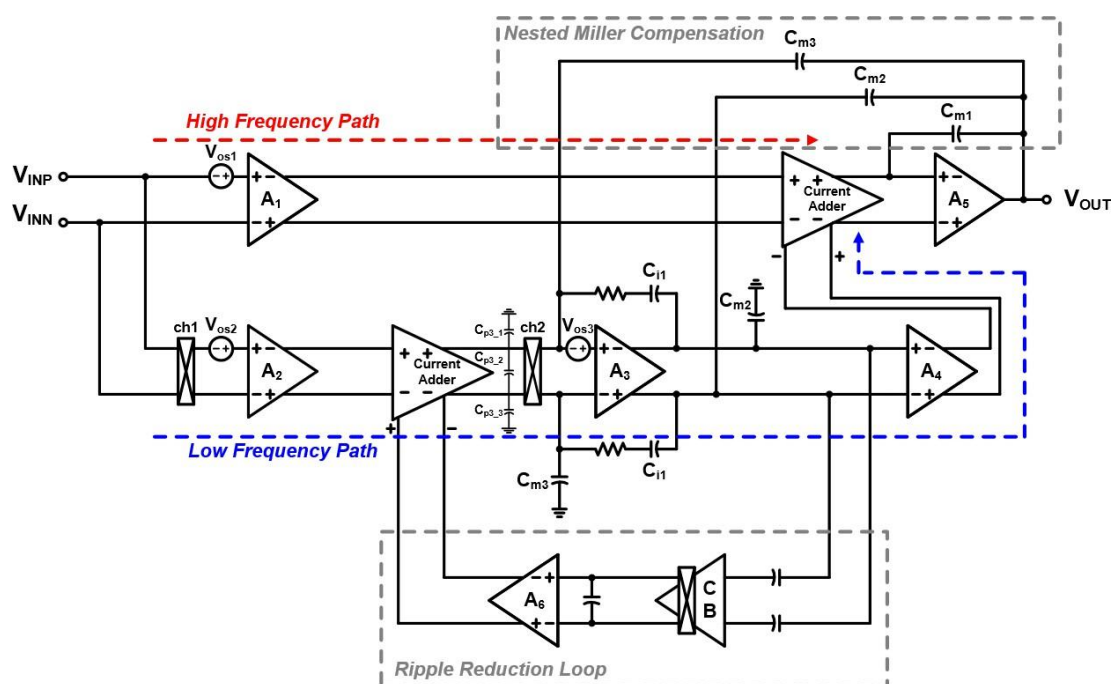


Figure 1. Block diagram of the proposed chopper-stabilized multi-path operational amplifier with nested Miller compensation.

2.2. Low-Frequency Path Design

The LFP is shown in Figure 2. Because the LFP amplifies in four stages and the HFP in two stages, the LFP predominantly determines the offset and flicker noise of the overall amplifier. Using the chopper, the offset and flicker noise are up-modulated to the chopper frequency to reduce the offset and flicker noise in the baseband. The schematic of the input stage is shown in Figure 3. The common mode feedback (CMFB) of the current adder is implemented with an amplifier structure. The V_{cmfb} is set to $1/2 V_{DD}$ so that the common mode voltage of the output V_{op} and V_{on} are set to $1/2 V_{DD}$.

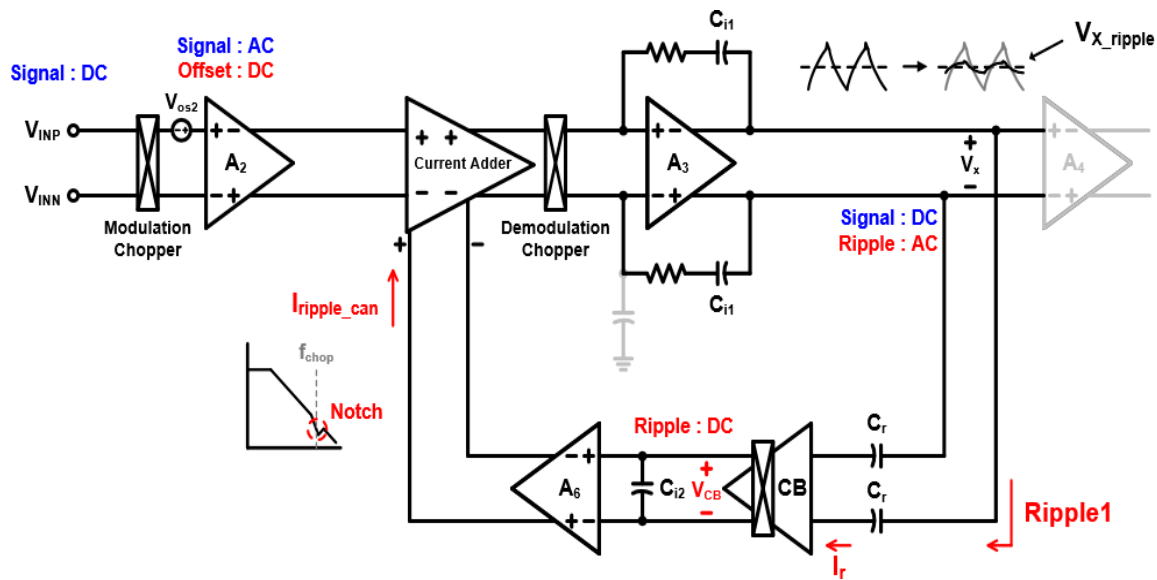


Figure 2. Simplified implementation of the low-frequency path (LFP) with the ripple reduction loop (RRL).

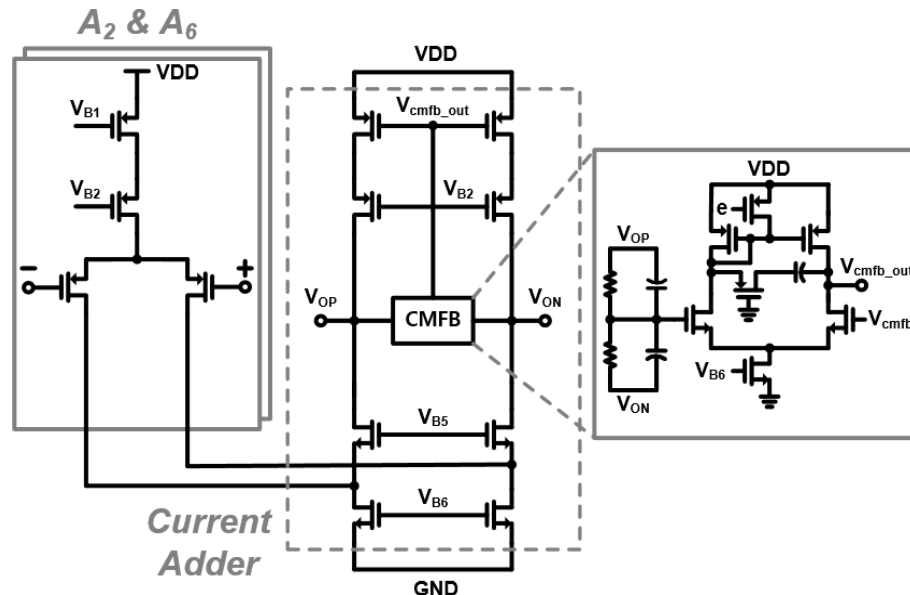


Figure 3. Schematic of the input stage.

The signal is converted to a current through A_2 and the ripple is converted to a current through A_6 . The two-signal current and the ripple current are subtracted through the current adder to suppress ripple. The output current of the current adder is converted to V_x through the A_3 integrator. V_x is converted to a current through A_4 and is merged with the HFP current through the current adder before A_5 .

2.3. Ripple Reduction Loop Design

The offset of A_2 is shown in V_x as the ripple due to the demodulation chopper and integrator A_3 . When the transconductance of A_2 is G_{m2} and the frequency of the chopper is f_{ch} , the ripple at the output of A_3 can be expressed as

$$V_{\text{ripple1}} \approx \frac{V_{\text{os2}} G_{m2}}{2C_{i1} f_{ch}} \quad (1)$$

When the transconductance of A_4 is G_{m4} , this ripple is integrated again by integrator A_5 so the ripple of the operational amplifier output can be expressed as

$$V_{\text{ripple2}} \approx \frac{V_{\text{ripple1}} G_{m4}}{8C_{m1} f_{ch}} \quad (2)$$

To reduce this ripple, the ripple reduction loop is used. The AC component V_{ripple1} is converted to the current I_r by the AC coupling capacitor C_r and is input into the current buffer (CB).

$$|I_r| \approx 2C_r f_{ch} V_{\text{ripple1}} \quad (3)$$

The CB is shown in Figure 4. If the output impedance of current source M_1 , M_2 , M_7 , and M_8 is large enough, the output voltage and DC output impedance of the CB are given in Equations (4) and (5). The A_{CB} is the DC voltage gain of the NMOS cascode in the CB. The output of the CB through A_6 is combined to estimate the amount of ripple suppressed by the current adder, as given by Equation (6).

$$V_{CB} = |I_r| \cdot R_{CB} \quad (4)$$

$$\text{where, } R_{CB} = \frac{A_{CB}}{2C_r f_{ch}} \quad (5)$$

$$I_{\text{ripple_can}} \approx \frac{A_{CB} G_{m2} G_{m6} V_{\text{os2}}}{2C_{i1} f_{ch}} \quad (6)$$

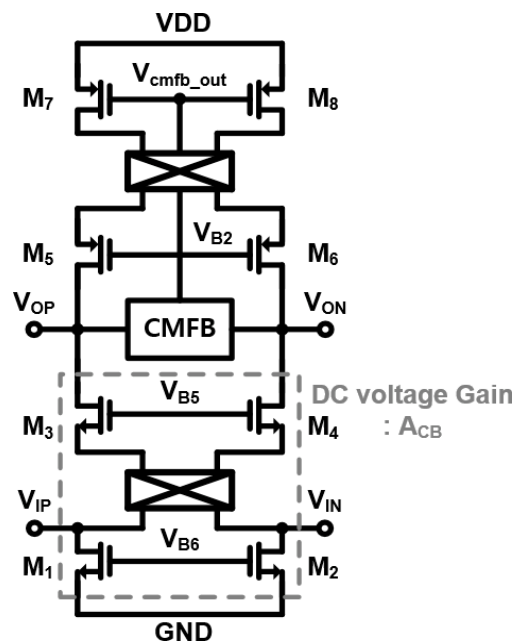


Figure 4. Schematic of the current buffer (CB).

The simulation results of the ripple for V_x when a 10-mV offset exists are shown in Figure 5. The red line is the output waveform of V_x in Figure 2 when RRL is not working, and the blue line is the

output waveform of V_x when RRL is operating. The ripple voltage was reduced by approximately 88%, from 68 mV to 8 mV by the RRL.

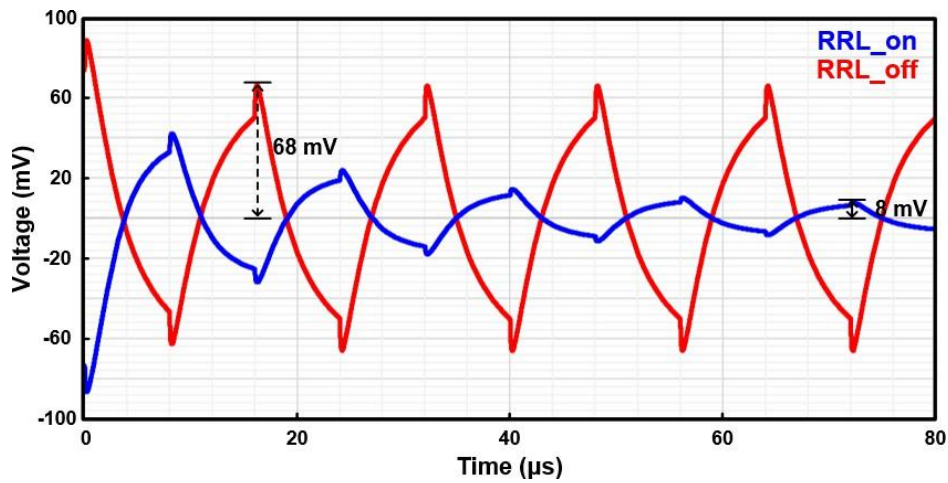


Figure 5. Simulation results of the ripple reduction loop.

Finally, the ripple suppression factor F can be expressed as

$$F = \frac{I_{\text{ripple_can}}}{I_{\text{os2}}} = \frac{A_{CB}G_{m6}}{2C_{i1}f_{ch}}, I_{\text{os2}} = V_{\text{os2}} G_{m2} \quad (7)$$

2.4. High-Frequency Path Design

The HFP of the proposed operational amplifier is shown in Figure 6. The HFP consists of a folded cascode and a Monticelli-class AB output circuit [12] to increase power efficiency. The HFP becomes active when the loop gain of the HFP exceeds the loop gain of the LFP.

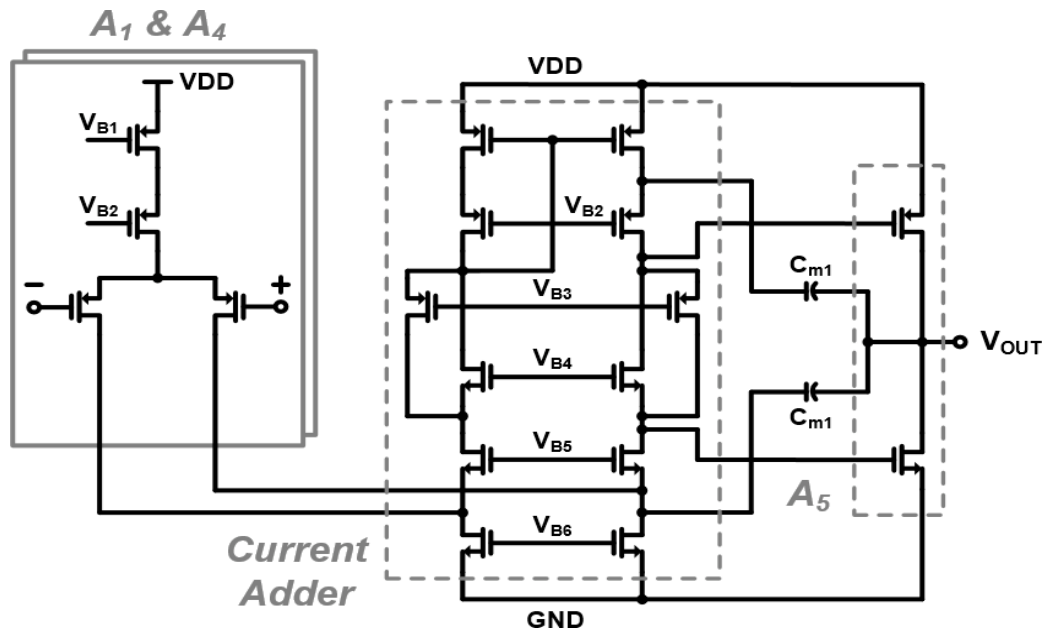


Figure 6. Schematic of the high-frequency path (HFP).

2.5. Frequency Response

The LFP and HFP signals are combined by the current adder in Figure 6. The LFP has a second-order frequency response caused by A_3 and A_5 and the HFP has a first-order frequency response caused by A_5 . To smoothly merge the transfer functions of the two paths, the frequency response of the LFP must be made similar to that of a first-order system. To accomplish this, the poles were split by applying the nested Miller compensation to C_{m1} , C_{m2} , and C_{m3} . In the case of C_{m2} , as there is positive feedback, there is a risk that the operation of the entire amplifier will become unstable by inducing the pole to appear in the right half of the complex-s plane [13]. Therefore, C_{m2} is connected to a negative terminal and its signal is implemented in the form of negative feedback.

The simulation results of the complete transfer function of the proposed operational amplifier are shown in Figure 7. The red line represents the HFP, the blue line represents the LFP, and the black line represents the overall transfer function of the multi-path operational amplifier. The frequency where the loop gain of the LFP and the loop gain of the HFP are equal is called the cross-over frequency and is determined by C_{i1} and A_4 in Figure 1. The overall transfer function follows the LFP function at low frequencies and the HFP function at high frequencies, and thus is not affected by the notch of the chopper frequency in the RRL. When the transconductance of A_2 is G_{m1} , the frequency response of the proposed multi-path operational amplifier is seen as the first-order frequency response, so unit gain bandwidth (UGBW) can be expressed as Equation (8). The simulation results show that the UGBW of the proposed multi-path operational amplifier is 2.2 MHz.

$$\text{UGBW} = \frac{G_{m1}}{2\pi C_{m1}} \quad (8)$$

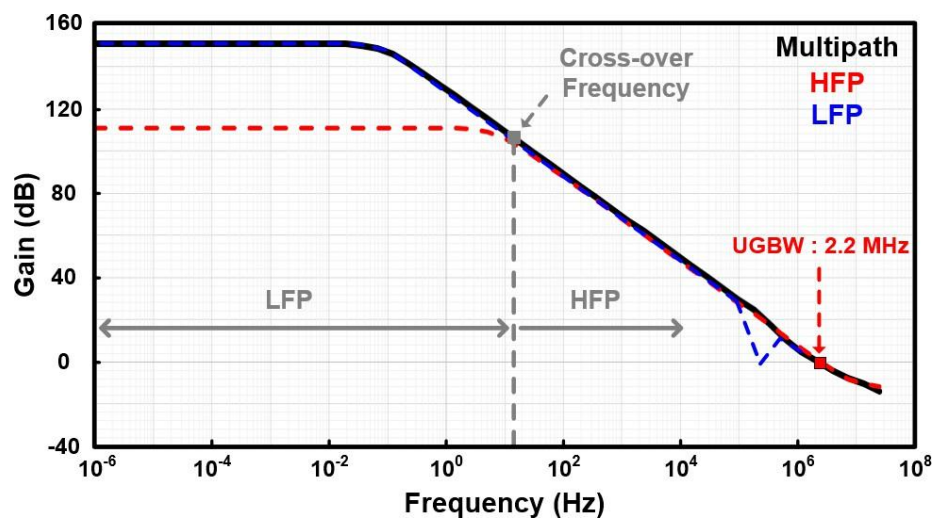


Figure 7. Simulation results of the proposed operational amplifier transfer function.

2.6. Residual Input Offset

In the case of LFP, the offset and $1/f$ noise were suppressed using the chopper and RRL. Depending on the ripple suppression factor F , the residual ripple can ideally be removed completely. In the case of HFP, since there is no chopper that suppresses the offset, the input offset is shown as the residual input offset. In terms of residual input offset, the offset V_{os1} of A_1 can be expressed as Equation (9) when the gain of HFP is A_{HFP} and the gain of LFP is A_{LFP} [14].

$$V_{\text{residual_input_offset1}} \approx \frac{A_{HFP}}{A_{LFP}} V_{os1} \quad (9)$$

The offset V_{os3} of A_3 also affects the residual input offset. V_{os3} is represented by a square wave by chopper ch2 and parasitic capacitor C_{p3_1-3} . The current to charge and discharge C_{p3_1-3} requires an input AC voltage of A_2 [14]. This AC voltage becomes the DC voltage via chopper ch1 and appears as the residual input offset, which can be expressed as

$$V_{\text{residual_input_offset2}} \approx \frac{4V_{os3}f_{ch}C_{p3}}{G_{m2}} \quad (10)$$

$$\text{where, } C_{p3} = C_{p3_2} + \frac{C_{p3_1} + C_{p3_3}}{2} \quad (11)$$

Chopper ch2 consists of 4 CMOS switches, as shown in Figure 8. Switching errors occur due to clock feedthrough caused by a mismatch of parasitic capacitors C_{p_ch21} and C_{p_ch23} in chopper ch2, which is seen as input offset [14]. C_{p_ch21} and the C_{p_ch23} are parasitic capacitors generated between the input of chopper ch2 and the switch gate. V_{clk} is the voltage of the clock signal. The residual input offset can be expressed as

$$V_{\text{residual_input_offset3}} \approx \frac{2\Delta C_{p_ch2}V_{clk}f_{ch}}{G_{m2}} \quad (12)$$

$$\text{where, } \Delta C_{p_ch2} = C_{p_ch21} - C_{p_ch23} \quad (13)$$

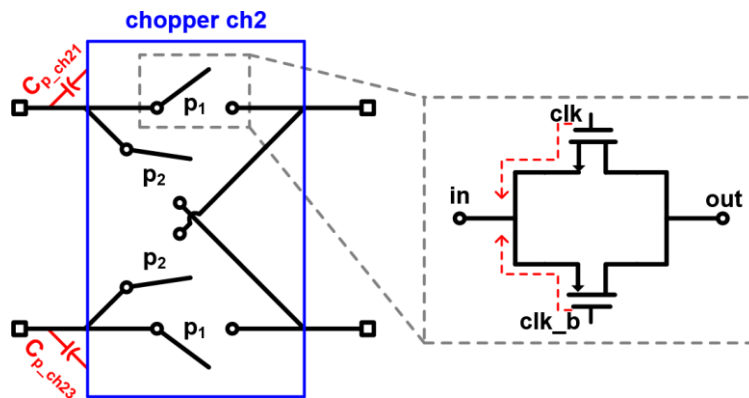


Figure 8. Schematic of chopper ch2.

3. Measurement Results

3.1. Chip Die and Measurement Environment

The proposed multi-path operational amplifier was fabricated using a standard 0.18- μm CMOS process. Figure 9 shows the die photograph and measurement environment of the proposed operational amplifier. The power consumption of the proposed low-noise operational amplifier is 0.174 mW with a 1.8-V supply and an active area of 1.18 mm^2 . The fabricated chip was connected to a printed circuit board for circuit performance measurements. A waveform generator provided clock and other input signals, and signal acquisition and data analysis were performed using a digital oscilloscope. A dynamic signal analyzer was used to analyze the spectrum.

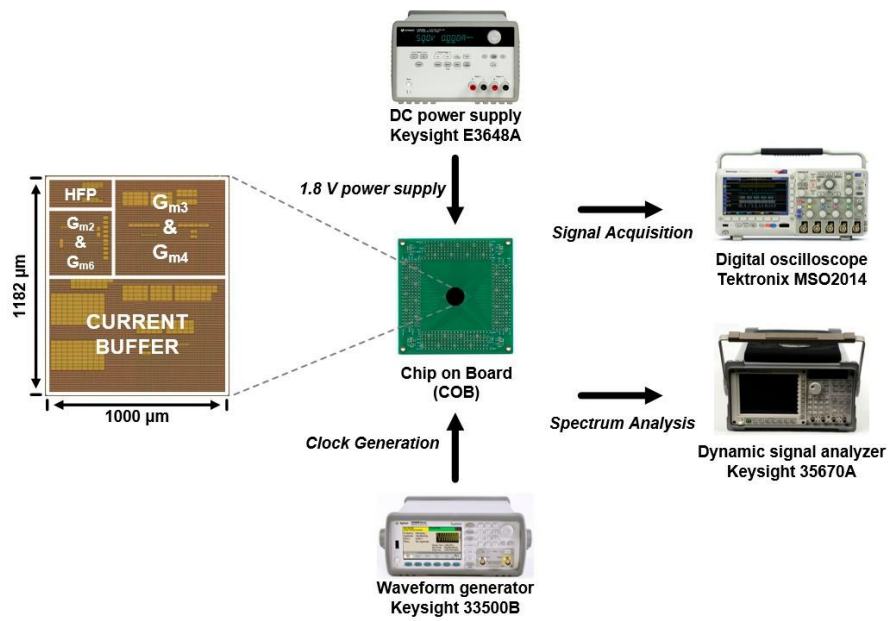


Figure 9. Die photograph and measurement environment of the proposed operational amplifier.

3.2. Measurement Results

The sine wave input and output and pulse wave input and output results for the buffer operation of the proposed multi-path operational amplifier are shown in Figure 10. The x-axis of (a) is 400-μs scale, the y-axis is 200-mV scale, and the x-axis of (b) is 2-μs scale, the y-axis is 50-mV scale. The red wave is the input and the blue wave is the output of the amplifier. Sinusoidal and pulse waves with an amplitude of 100 mV were applied using a 50-pF capacitive load. For the pulse response, the rise time was 1.15 μs.

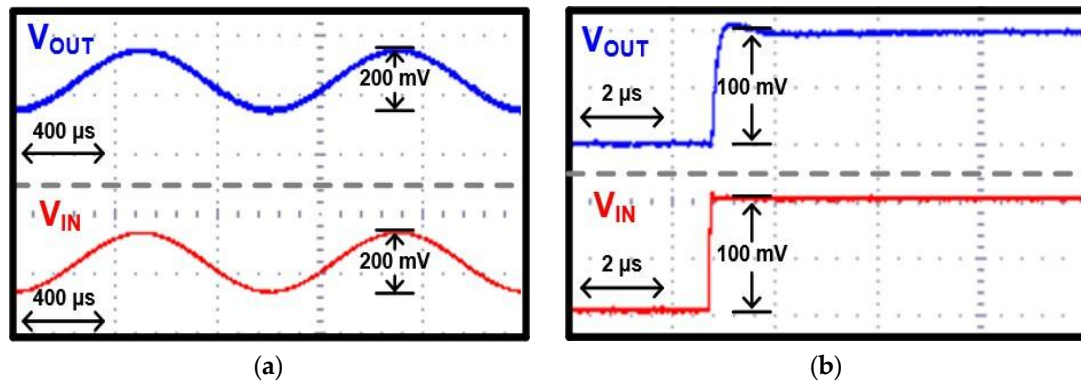


Figure 10. Measurement results of the buffer operation: (a) input sine wave and (b) input pulse wave.

The slew rate measurement results are shown in Figure 11. The red wave is the input and the blue wave is the output of the amplifier. The proposed multi-path operational amplifier exhibits a slew rate of 0.86 V/μs when a 1 V amplitude pulse wave is applied.

$$\text{Slew_Rate} = \frac{dV_o}{dt} = \frac{1V}{1.15\mu s} = 0.86V/\mu s \quad (14)$$

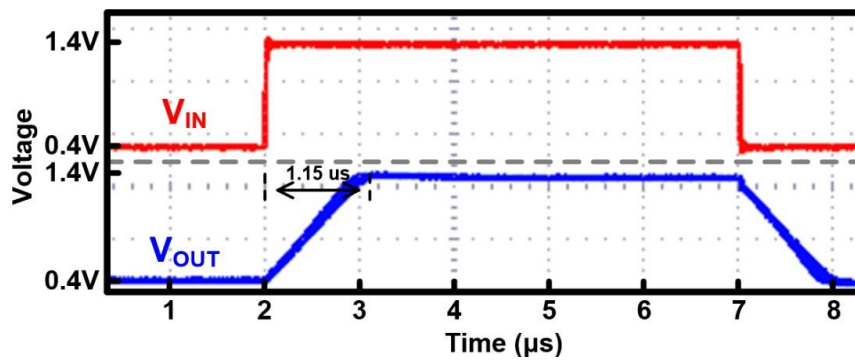


Figure 11. Measurement results of the slew rate.

Figure 12 shows the open loop gain measurement result of the proposed multi-path operational amplifier. The proposed operational amplifier has a gain of 135 dB at 1 Hz and exhibits a first-order frequency response. The proposed operational amplifier has a gain of 50 dB at 10 kHz and a unit gain bandwidth (UGBW) of 3.16 MHz. Compared with the simulation results in Figure 7, similar values are measured.

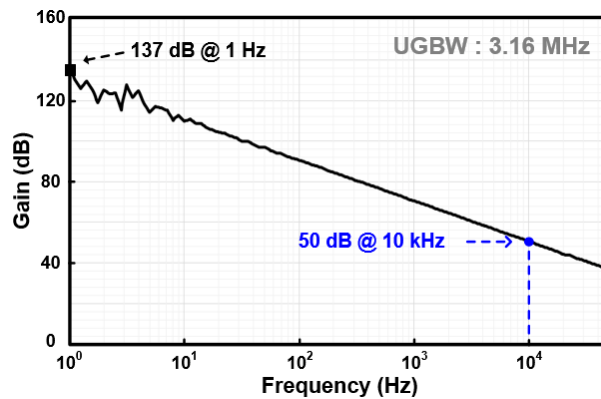


Figure 12. Open loop gain measurement results of the proposed multi-path operational amplifier.

Figure 13 shows the common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) measurements of the proposed multi-path operational amplifier. The proposed operational amplifier has a CMRR of 125 dB at 1 Hz and a PSRR of 100 dB at 1 Hz. The minimum values of the CMRR and PSRR are 69.8 dB and 71.7 dB.

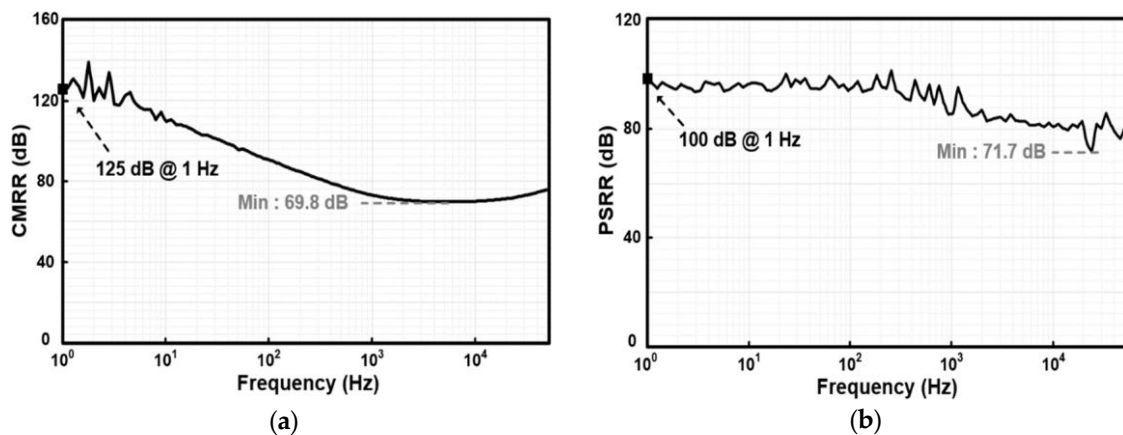


Figure 13. Measurement results: (a) the common mode rejection ratio (CMRR); (b) power supply rejection ratio (PSRR).

Figure 14 shows the results of the input referred offset measurement of the proposed multi-path amplifier. The input referred offset measurement shows that the average input offset is $1.99 \mu\text{V}$ and peak-to-peak offset is $3.73 \mu\text{V}$.

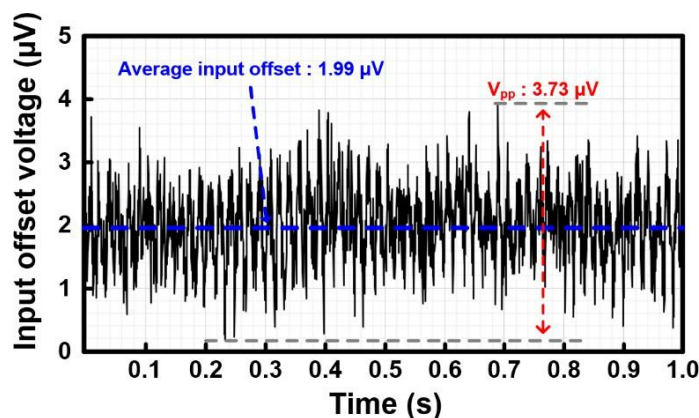


Figure 14. Input referred offset measurement result of the proposed multi-path amplifier.

The noise measurement results of the proposed multi-path operational amplifier for a bandwidth of 0.5–200 Hz are shown in Figure 15. Figure 15a shows the input referred noise of the proposed operational amplifier. The measured input referred noise is $47.8 \text{ nV}/\sqrt{\text{Hz}}$ at 1 Hz and $10.8 \text{ nV}/\sqrt{\text{Hz}}$ at 200 Hz. Figure 15b shows a noise histogram at 200 Hz for 10 samples. The average value of the input referred noise at 200 Hz for the 10 samples is $11.8 \text{ nV}/\sqrt{\text{Hz}}$.

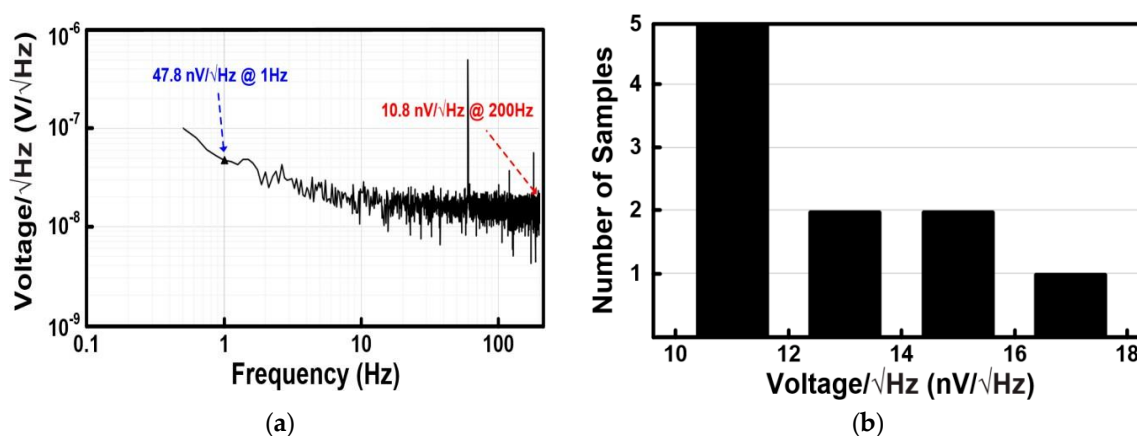


Figure 15. Noise measurement results of the proposed multi-path amplifier: (a) input referred noise and (b) histogram of the measured input referred noise at 200 Hz.

4. Discussion

A performance comparison with previous low-noise amplifier studies is shown in Table 1. When V_{ni} is the input referred noise and I_{tot} is the total consumption current of the operational amplifier, the NEF of the performance comparison can be obtained from Equation (15) [15]. The proposed low-noise chopper-stabilized multi-path operational amplifier achieves a current consumption of $96.7 \mu\text{A}$ with a 1.8 V power supply, UGBW of 3.16 MHz, and input referred noise of $11.8 \text{ nV}/\sqrt{\text{Hz}}$, resulting in a NEF of 4.46.

$$\text{NEF} = V_{ni} \cdot \sqrt{\frac{2I_{\text{tot}}}{\pi \cdot U_T \cdot 4kT \cdot \text{BW}}} \quad (15)$$

Table 1. Performance comparison: summary of measured parameters.

	This Work	[5]	[10]	[16]	[17]	[18]	[19]	[20]	[21]
Technology (μm)	0.18	0.18–0.5	0.7	0.7	0.3–0.6	0.35	0.18	0.18	0.32
Multi-path	Y	N	N	Y	N	Y	N	N	N
Power (μW)	174	25.9	1150	715	27	3675	74	3.24	561
DC gain	>137	168	-	100	>130	150	100	-	201.2
UGBW *	3.16M	260k	800k	1.8M	350k	4M	2k	-	40k
CMRR (dB)	>125	124	>120	137	-	-	>120	100	>120
PSRR (dB)	>100	120	>120	120	-	-	-	>70	115
Input referred offset (μV)	1.99	2	5	1	3	0.78	1.78	-	2
Input referred noise (nV/√Hz)	11.8	37	15	10.5	55	5.9	1.8	45.9	18
Chip Area (mm ²)	1.18	1.14	4.8	1.8	0.7	1.26	0.12	0.2	0.57
NEF **	4.4	5.5	8.8	4.8	8.1	8.4	17	2.37	10.6

$$\text{UGBW}^* = \text{unit gain bandwidth, NEF}^{**} = V_{ni} \sqrt{(2 \cdot I_{tot} / \pi \cdot U_T \cdot 4kT \cdot BW)}.$$

Because of the multi-path architecture, the proposed multi-path operational amplifier is relatively large in size and power consumption, but has a low input referred noise and wide bandwidth, so its NEF is better than previous studies.

5. Conclusions

This paper has presented a low-noise chopper-stabilized multi-path operational amplifier with nested Miller compensation for high-precision sensors. The proposed multi-path operational amplifier removes the offset, flicker noise, and ripple by applying a chopper stabilization technique and RRL, and enables wide bandwidth operation using a multi-path structure. Nested Miller compensation is applied to obtain the frequency response of a clean first-order system. The proposed multi-path operational amplifier was fabricated using a standard 0.18-μm CMOS process and an active area of 1.18 mm². The power consumption is 0.174 mW with a 1.8 V power supply. It achieves a slew rate of 0.86 V/μs, >137 dB open loop gain, >125 dB CMRR, and >100 dB PSRR. The NEF of 4.46 was obtained based on the achieved input referred noise of 11.8 nV/√Hz and UGBW of 3.16 MHz. The proposed low-noise multi-path operational amplifier has a good NEF and is suitable for precision sensor applications.

Author Contributions: H.K. (Hyoungcho Ko) conceived the study; H.K. (Hyungseup Kim), K.H., D.Y., H.H., Y.K., and D.C. designed the experiments; all authors participated in the tests and evaluations; J.K. wrote the paper. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflicts of interest.

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